Cost-Effective Smart Memory Implementation for Parallel Backprojection in Computed Tomography

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***Abstract*—As nanoscale lithography challenges mandate greater pattern regularity and commonality for logic and memory circuits, new opportunities are created to affordably synthesize more powerful smart memory blocks for specific applications. Leveraging the ability to embed logic inside the memory block boundary, we demonstrate the synthesis of smart memory architectures that exploits the inherent memory address patterns of the backprojection algorithm to enable efficient parallel image reconstruction at minimum hardware overhead. An end-to-end design framework in sub-20nm CMOS technologies was constructed for the physical synthesis of smart memories and evaluation of the huge design space. Our experimental results show that customizing memory for the computerized tomography (CT) parallel backprojection can achieve more than 30% area and power savings while offering significant performance improvements with marginal sacrifice of image accuracy.**

***Index Terms*—Smart Memory; Hardware Synthesis; Computed Tomography; Parallel Backprojection;**

I. Introduction

Computationally intensive algorithms in medical image processing (e.g., computerized tomography (CT)) require rapid processing of large amounts of data and often rely on hardware acceleration [1], [11], [2]. Inherent parallelism in the algorithms is exploited to achieve the required performance by increasing the number of parallel functional units at a cost of power and area. The overall performance is often defined by the limited bandwidth of the on-chip memory as well as the high cost of memory access.

One approach to address these challenges is to optimize the on-chip memory organization by constructing a customized smart memory module that is optimized for a particular function for higher performance and/or energy efficiency [14], [13]. However, such customization is generally unaffordable for an application-specific IC embedded memory for which cost dictates that it is "compiled" from a set of SRAM hard IP components (e.g., physical implementations of bitcells and peripheral circuits). Such memory compilation limits the possibility of application-specific customization and hinders the system design space exploration.

Recent studies of sub-20nm CMOS design indicate that memory and logic circuits can be implemented together using a small set of well-characterized pattern constructs [8], [9]. Our early silicon experiments in a commercial 14nm SOI CMOS process demonstrate that this construct-based design enables logic and bitcells to be placed in a much closer proximity to each other without yield or hotspots pattern concerns. While such patterning appears to be more restrictive to accommodate the physical realities of 14nm CMOS, the ability to make the patterns the only required hard IP allows us to efficiently and affordably customize the SRAM blocks. More importantly, it enables the synthesis (not just compilation) of customized memory blocks with user control of flexible SRAM architectures and facilitate *smart memory compilation.*

To efficiently leverage this new technology, however, algorithms and hardware architectures need to be revised. In this paper we revisit the well-known Shepp and Logan's backprojection algorithm that is widely used in the CT image reconstruction [2]. It is observed that in the parallel implementation of the algorithm, the memory address differences are fairly small for adjacent projection angles and adjacent pixels. We exploit this property via a customized memory structure that could feed in-parallel running image processing engines (IPEs) with a large amount of required projection data in one clock cycle. The implementation is realized by embedding "intelligent" functionality into the traditional interleaved memory organization and allow multiple memory subbanks to share the memory periphery. Novel periphery-sharing smart memory strategies are explored, and an efficient parallel-pipeline backprojection architecture is proposed. We further construct a smart memory design framework that provides the end user with finer control of the customized SRAM architecture parameters, thus enabling automatic generation of the specified implementation. Physical implementations were carried out in a commercial 14 nm SOI CMOS process. Our results indicate that there is more than 40% area savings and 30% power savings while providing significant performance improvements. The marginal impact on accuracy is minimized with appropriate constraints on the algorithm.

Related work. In other related work various fast approaches have been proposed to improve the backprojection implementation [11], [7], [6], [2]. As pointed out in [2], these approaches may be classified into three categories; namely, algorithmic improvement, dedicated hardware, and parallel processing. However, this paper shows that it is possible to combine these three aspects to deliver a more efficient backprojection architecture by taking advantage of the availability of smart memory synthesis. Our approach optimizes the parallel backprojection architecture, especially the on-chip memory architecture, by exploiting the inherent memory address pattern that has not been previously explored.

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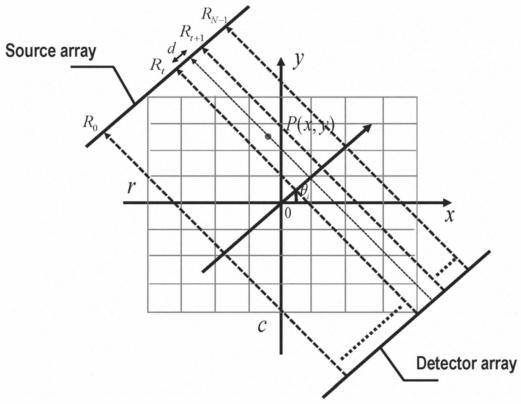

Fig. 1. Illustration of Parallel-Beam Projection: The object to be scanned is placed between the evenly spaced array of an unidirectional X-ray source and the detector. Radiation beams from the X-ray source pass through the object and are measured at the detector, forms the projections of the image.

II. ADDRESS PATTERN EXPLORATION

In a parallel-beam CT scanning system, as shown in Fig. 1, the object to be scanned is placed between the evenly spaced array of an unidirectional X-ray source and the detector. Radiation beams from the source pass through the object and are measured at the detector. A complete set of projections is obtained by rotating the arrays and taking measurements for different angles over $180°$, forming the Radon transform of the image (i.e., projection data). The inverse of the projection data allows to reconstruct the tomographic images (i.e., backprojection) [12], [1].

Shepp and Logan backprojection algorithm. The Shepp and Logan backprojection algorithm is the most well-known backprojection algortithm [2], [3]. For each pixel, P located at (x, y), and each projection angle θ_i, the first step in backprojection is to locate the pixel in an appropriate beam (ray). If the center of P is not on a ray, the distance (d) to its adjacent rays is calculated and the contribution from the adjacent rays to the pixel (Q_p) is computed according to the linear interpolation equation (1), assuming that pixel is enclosed by the t_{th} and $(t+1)_{th}$th rays,

$$Q_p(x, y, \theta_i) = R_t + (d/L) \cdot (R_{t+1} - R_t), \tag{1}$$

where R_t is the value of t_{th} ray, d is the interpolation distance, and L is the ray interval. Q_p represents the contribution of the projection angle θ_i to the current pixel value.

In the above equation, the address t to the projection data memory and the interpolation distance d are computed as follows (assuming the target image has the dimension size of $r \times c$):

$$t_{x,y,\theta_i} = \big(x - \frac{r}{2}\big) \cdot \cos\theta_i - \big(y - \frac{c}{2}\big) \cdot \sin\theta_i + t_{\text{offset}}. \tag{2}$$

$$d = t(\theta) - \lfloor t(\theta) \rfloor. \tag{3}$$

Address difference. The above procedures are to be repeated for every angle and for every pixel, which involves significant address computation and memory access operations. However, these operations can be simplified by the observation that the address differences for adjacent pixels and angles are within a very small and predictable range. To illustrate this inherent address pattern, we show the address to the next projection of angle θ_{i+1} in (4):

$$t_{x,y,\theta_{i+1}} = \big(x - \frac{r}{2}\big) \cdot \cos\big(\theta_{i+1}\big) - \big(y - \frac{c}{2}\big) \cdot \sin\big(\theta_{i+1}\big) + t_{\text{offset}}. \tag{4}$$

The address difference (δt_1) between (2) and (4) could be as

$$\delta t_1 = \big(x - \frac{r}{2}\big) \cdot \delta cos_{\theta_i} + \big(\frac{c}{2} - y\big) \cdot \delta sin_{\theta_i}, \tag{5}$$

with $\delta cos_{\theta_i} = \cos(\theta_{i+1}) - \cos(\theta_i)$ and $\delta sin_{\theta_i} = \sin(\theta_{i+1}) - \sin(\theta_i)$. Using trigonometric identities, we can compute the bounds on (5) as follows (assuming $r = c$ and N is the total number of projections):

$$|\delta t_1| \leq |2 \cdot \sin\big(\frac{\pi}{N}\big) \cdot \frac{r}{2} \cdot \big(\cos\big(\frac{\pi(2i+1)}{N}\big) - \sin\big(\frac{\pi(2i+1)}{N}\big)\big)|. \tag{6}$$

(6) has a maximum bound of $\sqrt{2}\pi \cdot \frac{r}{N}$ for relatively large N. This shows that δt_1 is limited to a fairly small range when the appropriate ratio of r and N is selected. For example, the value is always less than one when $\frac{r}{N} \leq \frac{1}{8}$.

This observation can easily extend to two scenarios below: (a) The address difference between the next k projection memory of angle θ_k and the first memory of angle θ_1 for the same pixel $P(x, y)$ will increase proportionally to k:

$$|\delta t_k| = |t_{x,y,\theta_{i+k}} - t_{x,y,\theta_i}| \leq \sqrt{2}\pi \cdot \frac{r}{N} \cdot k \cdot \approx 4.44 \cdot \frac{r}{N} \cdot k. \tag{7}$$

(b) The address differences when both pixel coordinate and projection angle are incremented are also bounded by a limited range. For demonstration purpose, we define the problem as to reconstruct four neighborhood pixels in parallel, that is, $(x,\ y)$, $(x+1,\ y)$, $(x,\ y+1)$, $(x+1,\ y+1)$. Then, their addresses in adjacent k projection memories for angles from θ_i and θ_{i+k} need to be computed. We denote the address of the first pixel $(x,\ y)$ in the first memory θ_i as the reference address ($t_0 = t_{x,y,\theta_i}$). Then we can easily prove that other addresses are all very close to t_0 for the required k, and the maximum possible address difference to t_0 is introduced by the last pixel $(x+1,\ y+1)$ in the last projection memory θ_{i+k},

$$\delta t_{max} = t_{x+1,y+1,\theta_{i+k}} - t_{x,y,\theta_i} = \cos\theta_i + \sin\theta_i + k \cdot \delta t_1. \tag{8}$$

It is easy to show that (8) has the maximum value of $\sqrt{2} + 4.44 \cdot \frac{r}{N} \cdot k$ and it is limited to small range, e.g., the value must be less than four when $\frac{r}{N} \leq \frac{1}{8}$ and $k = 4$.

The basic idea is, since the address differences for adjacent projections angles and adjacent pixels are small, these addresses will activate the same or adjacent wordlines when such memories are located horizontally in parallel with each other. It leads to opportunities to share the memory decoder among these memories by programming extra "intelligent" logic functionalities into the memory periphery.

III. SMART MEMORY CUSTOMIZATION FOR PARALLEL BACKPROJECTION ARCHITECTURE

In this section, we describe our approach to optimize the memory organization and backprojection architecture based on the observed memory access patterns.

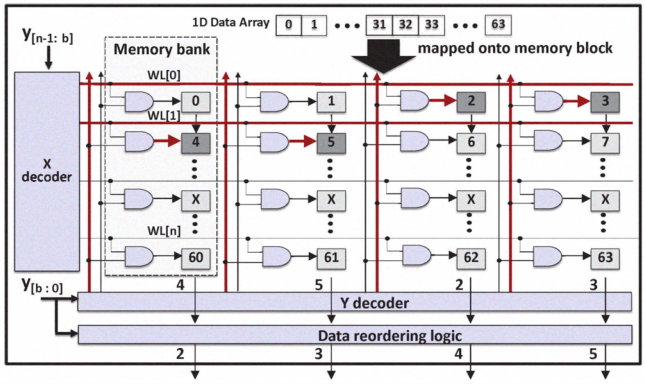

Fig. 2. Consecutive Access Memory. As the basic memory structure in the paper, our customized memory can output consecutive memory entries in one clock cycle and allows parallel memory banks to share the x-decoder.

A. Consecutive Access Memory

As we mentioned, linear interpolation is an important procedure of the algorithm. Linear interpolation requires the access to two adjacent array addresses of the projection memory in a single clock cycle. In our previous work [15], we have proposed a *rectangular-access smart memory* which is able to output an arbitrary rectangular block in a 2D data array. Its $1D$ simplified version, called $1D$ *Consecutive Access Memory*, can be used to output consecutive elements from a $1D$ data array. The functionality is defined as to support single-clock-cycle access of 2^b data points from a 2^n size data array. We build a parameterized memory which is first divided into 2^b memory banks and these memory sub-banks are located horizontally parallel to each other. Fig. 2 shows the organization of the memory block when $n = 6$ and $b = 2$. The main idea is to let these 2^b memory banks share one modified X-decoder. The X-decoder is specifically designed to activate two adjacent wordlines simultaneously (e.g.,$WL[0]$ and $WL[1]$). Another Y-decoder is used to select one of the two activated wordlines for each memory bank with the additional AND operations. This consecutive access memory serves as the basic memory structure in our method. In the rest of paper, we will propose more advanced memory sharing strategies customized for backprojection algorithms.

B. Smart Memory Organization and Parallel Backprojection

We will use a simple example to show the basic idea of the method. From the analysis of equation (6), we have derived that the address difference of the two adjacent memories (δt_{θ_1}) is less than one when $\frac{r}{N} \leq \frac{1}{8}$. This implies that the two adjacent memory addresses after rounding must be either the same or adjacent to each other. In Fig. 3, we show the physical data layout in our consecutive access memory. If the address of projection θ_i is located in between t_2 and t_3 (denoted by $[t_2, t_3]$), then the address in the next adjacent projection θ_{i+1} for the same pixel has only three possible locations, that is, $[t_1, t_2]$, $[t_2, t_3]$ or $[t_3, t_4]$. In the illustration we highlight the corresponding active wordlines if implemented in the consecutive access memory. It's seen that if the active wordlines for the first memory are wl_1 and wl_2, then in the next memory, the active wordlines must be either the same (wl_1 and wl_2) or

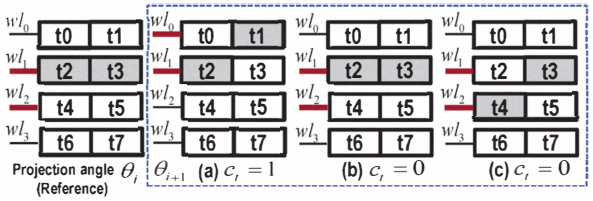

Fig. 3. Data Layout in Adjacent Two Projection Memories. If t_2 and t_3 are required in the first reference memory of the projection θ_i, then beam pixel required in the next memory of projection θ_{i+1} has three possible locations, that is, $[t_1,t_2]$, $[t_2,t_3]$ or $[t_3,t_4]$.

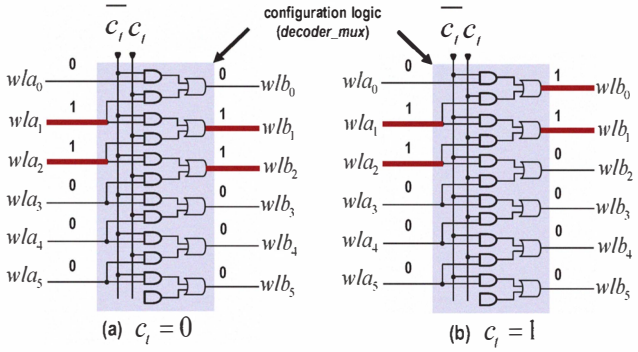

Fig. 4. Decoder-MUX. The wordlines of the first memory (wla_i) are configured to generate the wordlines for the next memory (wlb_i), so that the decoder of the latter memory could be eliminated.

shifted upwards by one step (wl_0 and wl_1). We use a control signal c_t to differentiate these two situations and c_t can be calculated from the input address. Based on this observation, we propose two "smart" memory approaches which are named *decoder-mux* and *output-mux* respectively.

Decoder-mux. In the first approach, called *decoder-mux*, we eliminate the decoder of the second memory and let it share the same decoder with the first memory by adding some configuration logic (which we also call decoder-mux) in between the two sets of memory wordlines. This logic configures the wordlines of the first projection memory (wla_i) to generate the wordlines for the next adjacent projection memory (wlb_i). The relationship between the wordlines of the two adjacent memories can be derived as

$$b_i = (-c_t) \cdot a_i + c_t \cdot a_{i+1}. \tag{9}$$

The configuration can be implemented using only AND and OR logic gates, which ensures the feasibility of the hardware implementation. In Fig. 4, we show an example of the configuration logic involving six wordlines. In this example, wla_1 and wla_2 are activated in the first memory array. After the decoder-mux block, either the same wordlines, wlb_1 and wlb_2, are activated in the second memory when $c_t = 0$ (Fig. 4(a)), or the neighborhood wordlines, wlb_0 and wlb_1, are activated when $c_t = 1$ (Fig. 4(b)).

Output-mux. In the alternative approach named *output-mux* the two memories still share the decoder but the configuration logic is located outside of the memory (see Fig. 5). In this approach, memories are designed as the 1×4 consecutive access memories to output more elements than required. In this example, t_2, t_3 along with their nearest neighbors t_1 and t_4 are all read out from the memories. Then the configuration logic

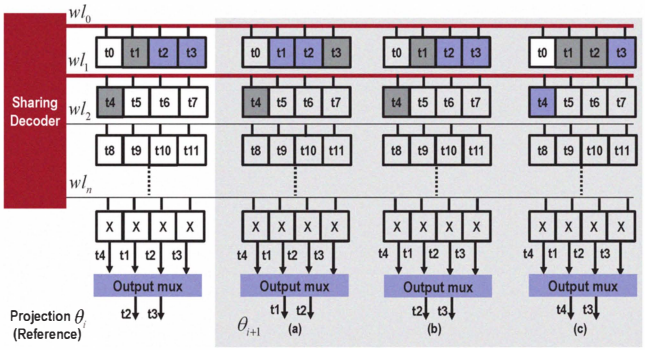

Fig. 5. Output-MUX. The memories are configured to output four pixels simultaneously, and the *output mux* is used to select the required two pixels from the four outputs for the liner interpolation in each backprojection.

(*output-mux*) is used to select the appropriate two elements from the four outputs. In this approach, the active wordlines for the two memories are always the same in all the situations.

Horizontal and vertical parallel backprojection. The CT image reconstruction naturally lends itself to parallel processing since each backprojection can be processed independently. However, in the conventional parallel backprojection, on-chip memory is typically divided into many small banks to support the necessary large data bandwidth. To exploit the proposed smart memory to obtain superior hardware efficiency of the parallel backprojection, we propose two parallel approaches, *horizontal and vertical parallel backprojection.*

The horizontal parallel backprojection can perform more than two backprojections in parallel and all the involved projection memories share the same memory decoder using either *decoder-mux* or *output-mux* approach. Fig. 6 shows the example of accessing in eight adjacent projection memories. Assuming that the pixels addressed by the first memory addresses are t_3 and t_4, we highlight the possible locations of the two pixels accessed in the next seven memories. We observe that they are all clustered locally around t_3 and t_4, and are bounded by t_0 and t_7. For example, the pixels required for projection θ_{i+3} could be any two adjacent pixels within $[t_1, t_6]$. Required pixels spread out further from t_3 and t_4 for memories that are further away from the first memory as explained by formulae (7), as the address difference of the next k projection memories from the first reference is increasing proportionally with k. Similar to the *output-mux* design shown in Fig. 5, we configure each projection memory as an 1×8 consecutive access memory to output all the shown eight pixels and use another 8-to-2 output-mux to select the appropriate two outputs from the eight outputs for each projection memory. In this way, all the eight memories could share the same decoder and seven memories decoders are saved. However, as the projection memories output more pixels than required, many memory outputs are actually wasted. An approach to use these wasted pixels is applying vertical parallel backprojection, as discussed next.

Vertical parallel backprojection is performing the backprojections of multiple neighborhood pixels in parallel. E.g., in equation (8) we discuss the address differences for performing the backprojections of four neighborhood pixels concurrently.

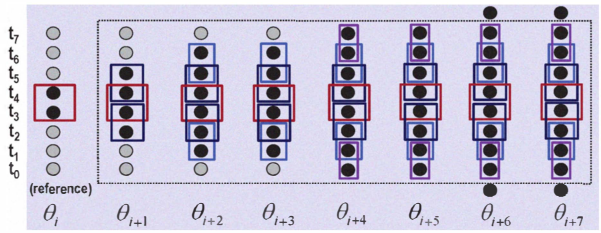

Fig. 6. Parallel Projection Memory Accessing. The highlighted two-pixel groups represent the beam pixels that have chances to be accessed in each

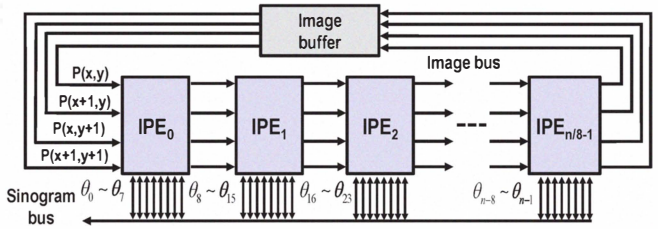

Fig. 7. Backprojection Architecture. Each IPE stores and performs eight backprojections for four neighborhood pixels concurrently.

Backprojection of each pixel per projection angle requires one linear interpolation and involves memory accessing of two pixels, so totally it requires eight pixels to be accessed from each projection memory. (8) shows that these eight pixels will be contained in the outputs of the above 1×8 access memory in most situations. Therefore, the memory architecture needs no change for the vertical parallel backprojection since we just take advantage of the unused memory outputs from the horizontal parallel backprojection. By implementing both horizontal and vertical parallel backprojection concurrently using the modified consecutive access memory, all the memory outputs are utilized and a much higher throughput is achieved.

Advanced parallel pipeline backprojection engine. Based on our proposed horizonal and vertical backprojection methods we designed an Advanced Parallel Pipeline backProjection Engine (APPPE) based on the Parallel Pipeline backProjection Engine (PPPE) that was proposed in [5], [1]. APPPE is composed of a pipeline of identical image processing engines (IPEs), where each IPE performs multiple backprojections to multiple pixels concurrently. Fig. 7 shows an example where the input image passes through the IPEs on the pipelined image bus, four pixels at a time. Each IPE_i in the pipe performs eight adjacent backprojects from θ_i to θ_{i+7} to the current four pixels $(P(x,y), P(x+1,y), P(x,y+1), P(x+1,y+1))$, and then passes these pixels onto the IPE_{i+1} as it receives another four pixels from IPE_{i-1}. As these pixels are sent through the pipelined array, the pixel values are accumulated from the contributions of all the projections.

IV. DESIGN AUTOMATION

In this section we analyze the design space and describe our design automation framework for the hardware synthesis of a user-specified backprojection design point.

Design tradeoff space analysis. Designing a CT image reconstruction system is a tradeoff problem involving algorithmic constraints, performance, hardware cost, and image accuracy. The discussion of address patterns in Section II shows that the ratio of image dimension size (r) and the

projection numbers (N), r/N, is an important algorithm constraint. Smaller r/N indicates smaller adjacent address differences, which allows for more adjacent projection memories sharing the memory decoder, saving more hardware cost and computing latency. However, it also limits the use of the method in applications with larger image size r and/or fewer projection angles N. For larger r/N, the corresponding larger address difference will limit the number of projection memories that can share the decoder. For example, in Fig. 6, the last two projection memories of θ_{i+6} and θ_{i+7} may require to access two pixels at the two ends, which are not accessible along with other eight pixels from the 1×8 consecutive access memory. To solve this problem we could increase the memory access width and apply more complicated configuration logic. However, this would increase the hardware cost. Alternatively, to lower hardware cost we could assign the nearest neighborhood pixels if the requested pixels are not available, which would result in loss of image accuracy. This shows that different design decisions will result in different tradeoffs. The combination of these design choices constitutes a huge design space. Further, exploring the design tradeoff space requires customized memory designs, which are traditionally prohibitively expensive. Thus, a strong design automation tool is required to make the hardware synthesis feasible.

End-to-end smart memory design framework. We have developed a *smart memory design framework* that provides designers with a graphical user interface to select design parameters, and automatically generate the optimized smart memory hardware IP [14], [13], [15]. As shown in Fig. 8, the tool frontend is built using the chip generator infrastructure "GENESIS" [10], [4]. It provides a user-configurable graphical interface that allows the user to input design specification and generates the optimized RTL automatically. The tool backend is a *smart memory compiler* for the physically synthesis of customized smart memory, which is developed based on the logic and memory co-design methodology [8], [9], [15]. Using this tool, embedded random logic and memory periphery are synthesized with the memory cells one shot to a small set of pre-characterized layout pattern constructs. Lithographic compliance between the co-designed logic and memory ensures the sub-20nm manufacturability of smart memory blocks. The architectural frontend and physical backend is combined to build an end-to-end smart memory design framework. Its input is the design specification and the output is the ready to use hardware (RTL, GDS, .lib, .lef).

V. EVALUATION AND RESULTS

In this section, we evaluate the smart memory architectures with respect to area, power, latency, and accuracy. The design framework is used to generate various design points. Area and power are measured from the physical implementations of the design on a commercial 14 nm SOI CMOS process at 500MHz and the shown results are all normalized.

Cost evaluation. In Fig. 9 (a), we first compare the hardware cost of two smart memory approaches (*decoder-mux* and *output-mux*) to the conventional memory approach where

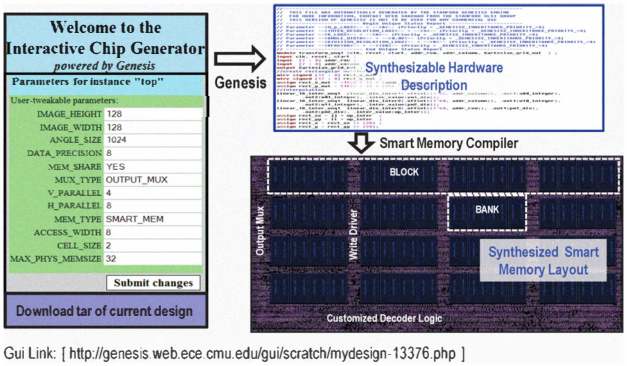

Fig. 8. Smart Memory Design Framework

each memory has its own decoder. The memories studied here have the size of 4,096-words and wordlength of 16 bits, and we only consider two memories implemented as 1×8 consecutive access memories sharing the decoder with each other. We observe that the *output-mux* approach is more cost-efficient as saves around 30% area and 20% power while *decoder-mux* only achieves around 5% area saving and 10% power saving. The reason is that in *decoder-mux* each wordline is accompanied by a set of configuration logic (two AND gates and one OR gate), and each set of logic communicates with its local wordline. This explains also why *decoder-mux* achieves relatively higher power-efficiency compared to its area-efficiency. In contrast, *output-mux* only requires a single large configuration logic at the memory output while its memories have large access width as they output more pixels than required. Due to the superiority of the *output-mux* method, it will be used for our backprojection system in the following discussions.

In Fig. 9 (b) we evaluate the hardware cost of the MEPPPE memory architecture for reconstructing a 256×256-size image from 1,024 projections. The x-axis is the parallel degree P_d, which is defined as the number of adjacent backprojections that are performed in each IPE concurrently and its value varies from two to eight. In our implementation these P_d projection memories will all share the same memory decoder. The y-axis shows the relative area and power compared to the conventional design where no memory sharing strategies are used. We see that more than 40% area savings and more than 30% power savings can be achieved with the increase of P_d. Fig. 9 (c) shows that the latencies are decreasing proportionally with the increase of P_d as expected. Moreover, we achieve a four times performance improvement by computing four pixels in parallel in each IPE.

Accuracy evaluation. As we gain in both of hardware cost and performance, the effect on accuracy needs to be evaluated. We measure the mean square error (MSE) of the reconstructed image compared to the reference image and plot the results in Fig. 10 for parallel degrees (P_d) from one to eight. As expected, the error increases when either P_d or algorithm parameter (r/N) increases. This is because that we let P_d projection memories share the same memory decoder, and it will introduce error if the address differences of these P_d

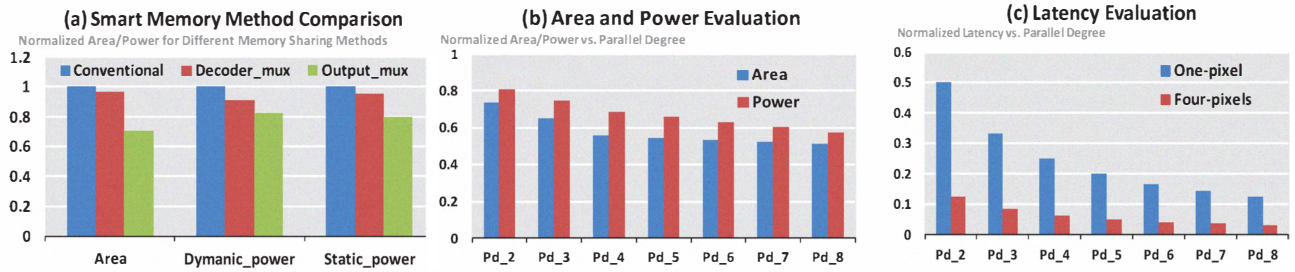

Fig. 9. Cost and Performance Evaluation

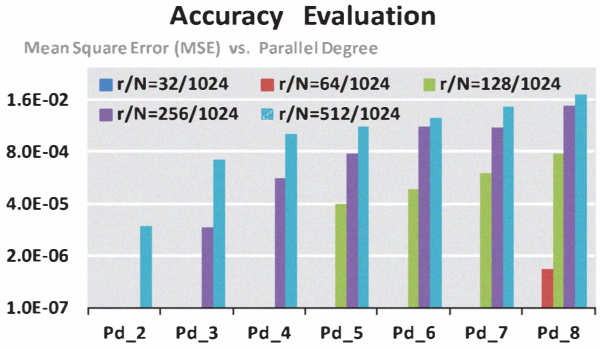

Fig. 10. Accuracy Evaluation

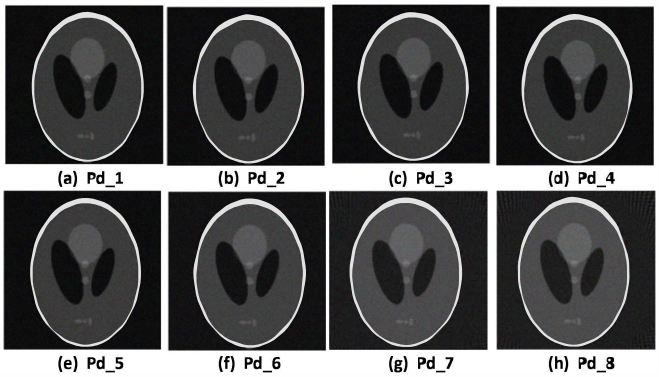

Fig. 11. Display of Reconstructed Image

projection memories are not small enough which could happen when P_d and (r/N) are large. In our implementation, we carefully manipulate the data precision so that the numerical errors can be ignored in the accuracy comparison. In Fig. 11 we display the reconstructed head phantom images from hardware simulation, which indicates fairly high image quality for all the studied parallel degrees. We also observe the gradual deterioration of the image quality for higher parallel degree, which allows us to tradeoff image accuracy with hardware cost in applications where minor distortion is acceptable.

VI. Conclusion

The emergence of construct-based design facilitates the robust synthesis of cost-effective smart memory blocks that are customized for specific applications. This cutting-edge design methodology creates opportunities to re-design algorithms and re-architect the hardware structure to match the advanced technology capabilities. In this paper we propose smart memory architectures and the end-to-end design framework to implement them for the CT image reconstruction problems. The results in a 14nm CMOS process demonstrate significant improvements in area, power and performance. Moreover, we present the opportunities to tradeoff hardware cost with acceptable image accuracy based on appropriate algorithm tuning. This paper demonstrates that the embedded memories in data-intensive computing can exploit the smart memory design methodology and the inherent address pattern of the algorithm to achieve superior power and performance efficiency.

Acknowledgement

The authors acknowledge the support of the C2S2 Focus Center, one of six research centers funded under the Focus Center Research Program (FCRP), a Semiconductor Research Corporation entity.

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